An analysis of the traditional QSD, and some improvements

1. Intro and background

The Quadrature Sampling Detector (QSD) has been well known for 10 years, and goes back to the early 1990s. Made famous by Dan Tayloe's patent and subsequent use by Flexradio and similar devices. The most popular kit sold was the Softrock series. I made a multi band Softrock type rig, but was not satisfied with the performance.

The Mobo 4.3 project was a system to make the SR V6.3 multi-band and give it a lot of other facilities. The design was ambitious, but fell down on many fairly small issues:

1. The PCB layout was compromised by having to fit onto the SR V6.3 board.
2. The PCB was only 2 sided and suffered a lot of spurs
3. Some questionable component choices

On the other hand the core technology, including the SDR-widget software and the adaptability of the whole thing was second to none. Eventually I may do a complete redesign, but for now this report represents a technology block. There is no point in just taking the original Mobo + SR V6.3 circuits and laying them out on 4 layer PCB. For starters, the Atmel USB controller is redundant. The main problem though is the SR V6.3 itself. To make a high performance receiver means designing it from end to end.

I looked at every block of the system, and found a satisfactory solution. The last one was the QSD. The Softrock QSD is a minimum cost implementation that has some flaws.

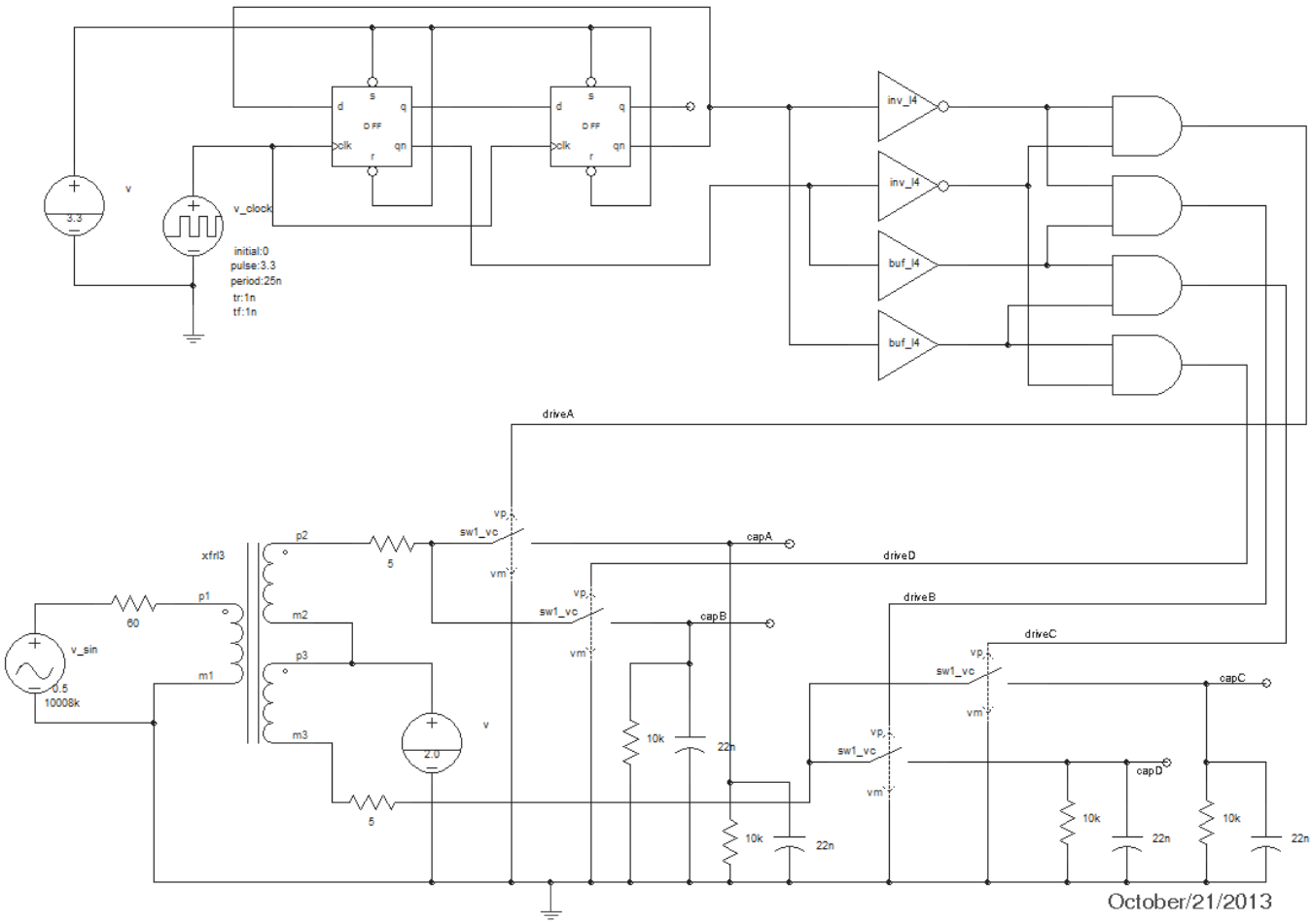
1. NMOS switches are running barely in conduction, with DC voltage at 2.5V
2. Switch chip and op-amps are DC coupled, so cannot be optimally biassed
3. Circuit is not double balanced and produces antenna radiation of the L.O.
4. Tolerance of components produce significant I/Q imbalances
5. Unbalanced output makes the notorious "DC spike" effect worse

There are many variants of the QSD to study. My eye fell on the balanced design, and on some newer chips to implement it with. It turns out that only 1 more dual op-amp is needed over the original SR6.3 circuit to produce a balanced version that should perform better. Alternatively a fully differential amplifier and options for output signal levels.

This document is a report mainly based on simulations using "Saber" from Synopsys. Garbage in garbage out with any simulation is true, but I don't think my results are fatally flawed. I was careful to include things like the transformer loss, and analog switch on-resistances, though I will concede that the exact transfer characteristic of the switches was too difficult to put in.

2. Single balanced SR V6.3 circuit

To begin there are some simulations of the original SR 6.3 waveforms. Circuit:



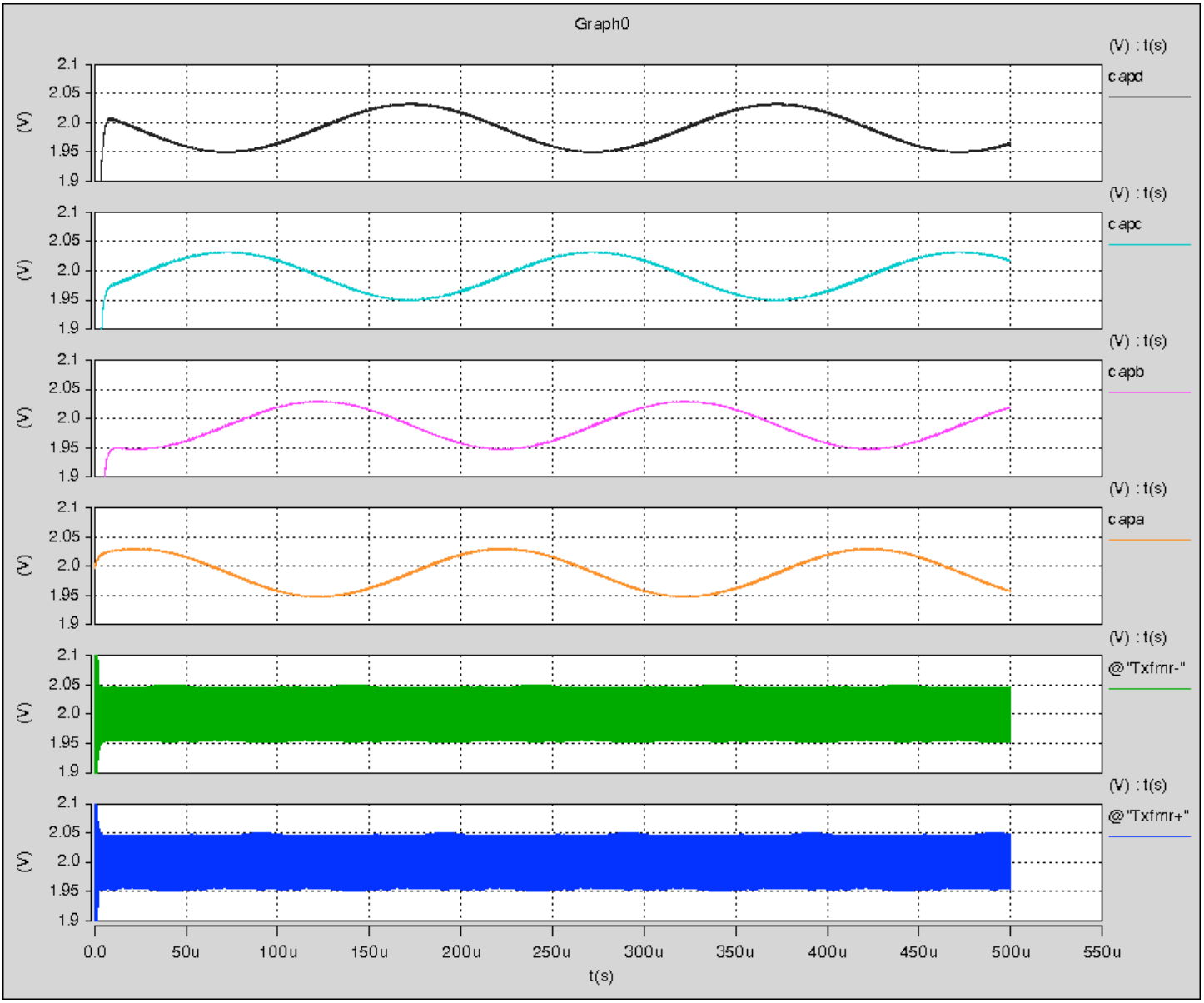
You will notice this doesn't look much like the SR V6.3 QSD circuit. The divide by 4 is recognisable on the top left. The buffer/NAND section top-right is actually what is contained in a typical 4:1 multiplexer. It produces a 1-of-4 pulse, hitting the switches sequentially. The switches in Saber can be modelled with most parameters of a real analog switch. It is difficult to model the conduction curve of an NMOS device accurately, and as I do not intend to use one in the final design, I didn't try to do that.

The input transformer winding is shown grounded. That is needed by Saber to converge the simulation. Otherwise it issues the notorious "Newton-Raphson" error. The transformer is a 1:1 with centre tap, so effectively 1:0.5.

It is well worth looking at the basics of the waveforms produced by this circuit. It does indeed give a low frequency signal when clocked at 4x the input frequency, with an audio range offset. In the following diagram, the signals on the 4 sampling caps (22nF) are shown. They are 90 degrees phase shifted, as expected. The green and blue bands show the incoming signal

voltages on either side of the input transformer. The input transformer loss was not fully characterised at this stage.

The 2.0V source at the centre of the transformer simulates a voltage divider. Normally this is two resistors plus a decoupling cap. But in the simulation the charging time of the decoupling cap makes a discontinuity, so the simulation needs settling time. Due to the computation time I removed the divider circuit, there will be no effect on the results from this. I later found a



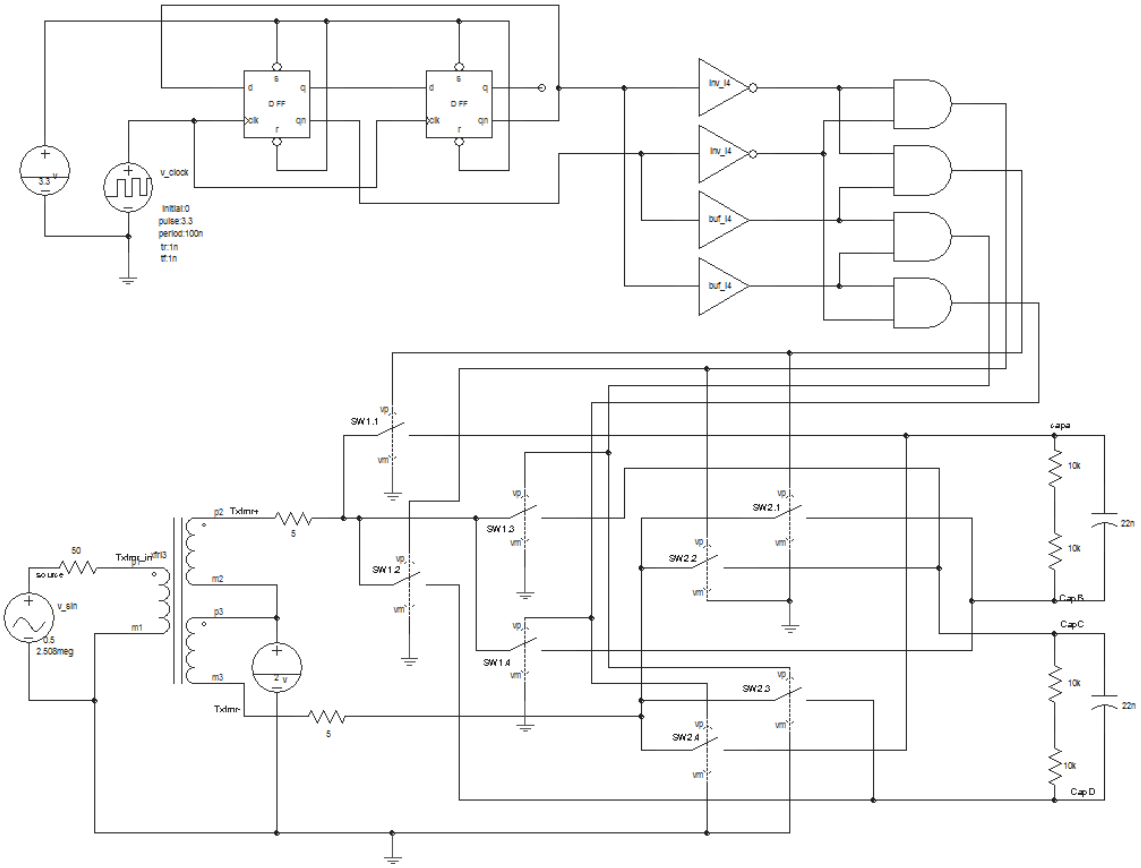
way to put a delay time into the simulation, and thereby overcome the startup anomaly. It is worth noting the transformer is simulated to the same turns ratio as the Softrock kit instructions. The voltage on the analog switches is about half that of the input.

The SR V6.3 circuit proved the basic simulation was running. Switching artefacts make the 4 lines on the results look thicker in the graph above. There are small pulses visible on each when magnified. Low pass filtering following can remove most of that. Changing the values of the non-linearity swamping resistors and the capacitors didn't make much difference until taken to extremes.

I intend to use polyester sample-hold caps instead of the ceramic ones, because they are tighter tolerance. Poly caps are shied away from in RF circuits generally, but there will be little genuine RF going through these. Besides the loss of poly caps above 10MHz may actually help a little with the filtering. 2%, 16V poly caps are easily available in 1206 packages.

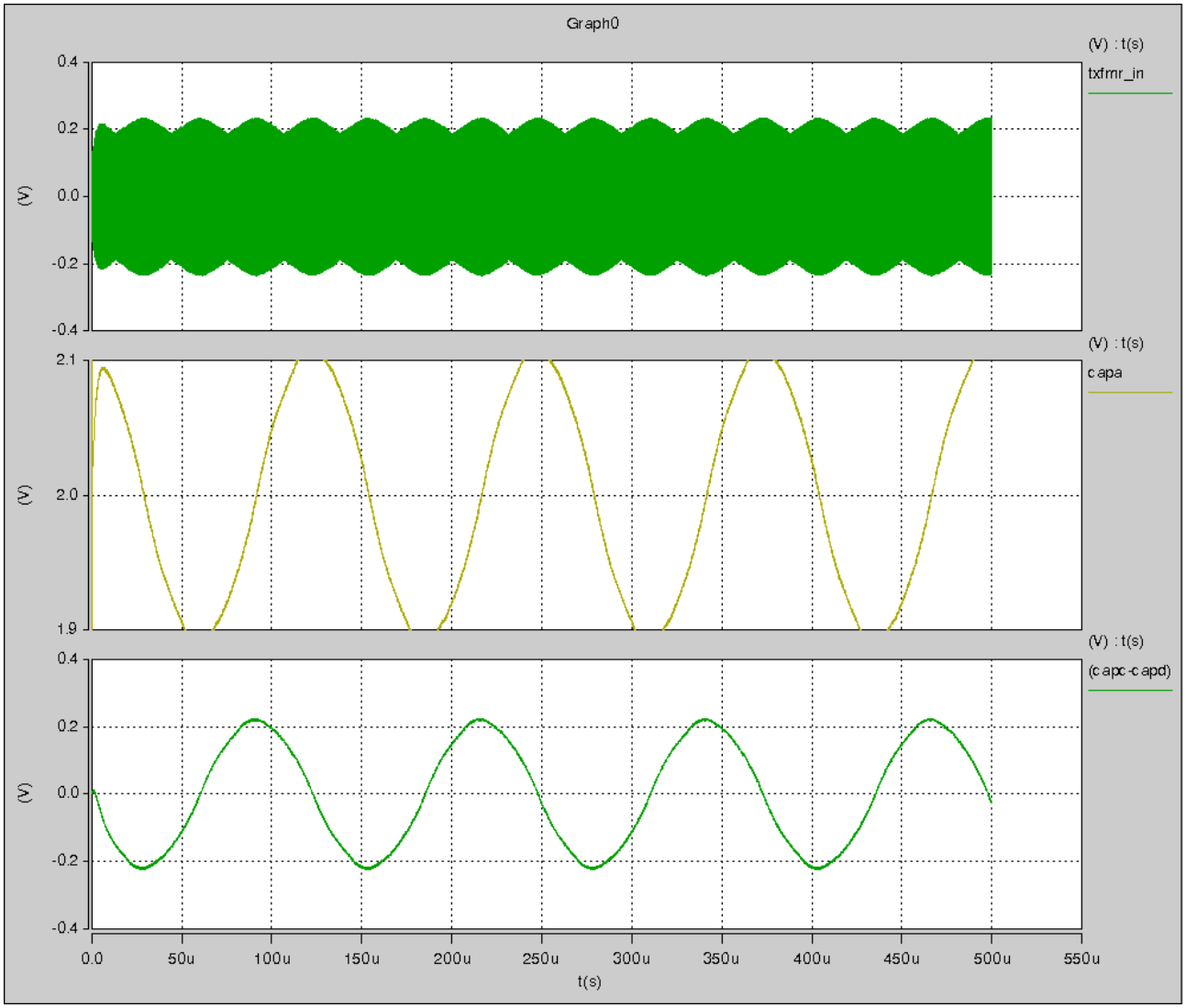
3. Double balanced simulation

My final target is to simulate the double balanced QSD. This uses 8 switches, but that is still only 1 actual chip. A beauty of the circuit is no more switch chips are needed. A simulation circuit for the double balanced version is a bit more complicated:



I am aiming for a balanced final output. So there is no need to have 4 sampling capacitors. One on each signal makes things better all round, saving 2 capacitors, and reducing the tolerance spreads of the circuit. The balanced design gives 3dB signal increase for free because both sides of the transformer are charging a sampling capacitor on all cycles, not half like the unbalanced version.

The next diagram shows input signal, voltage at one of the sampling caps, and differential result on the other sampling cap (using waveform calculator). The switch non-linearity swamping (a horrible phrase) resistors set at 10ohms. 10MHz digital clock and 2.505MHz in.

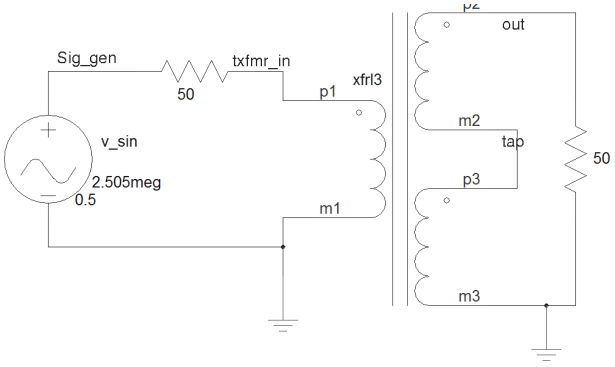


Next step is to check the voltages shown in the simulation reflect reality in transformer loss and the swamping resistor/switch combinations. This allows an estimate of gain for the subsequent amplifier, and optimisation of dynamic range.

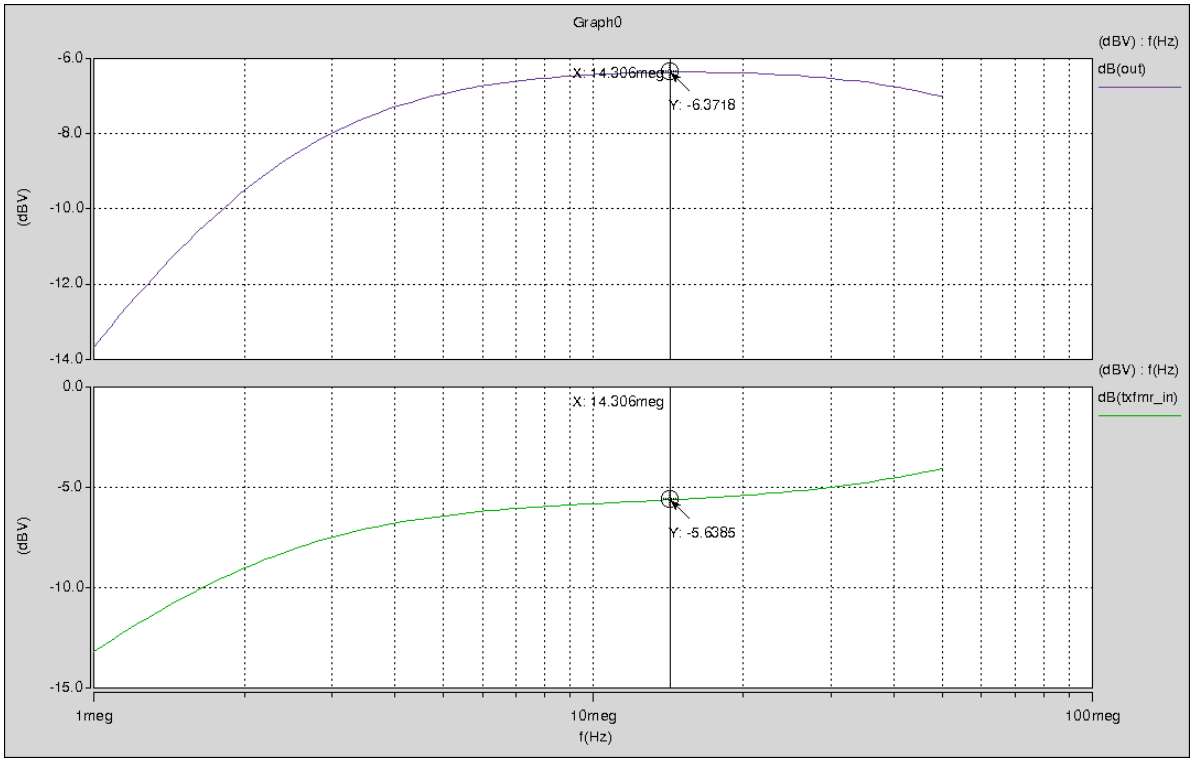
4. Simulation integrity and Differential amplifier

The transformer model in Saber gives a more realistic result when setup in terms of magnetic path length and path distance. The model also includes permeability of the core, and additional coupling factors. Of course turns ratio too.

Looking at the transformer on it's own with the following small circuit.

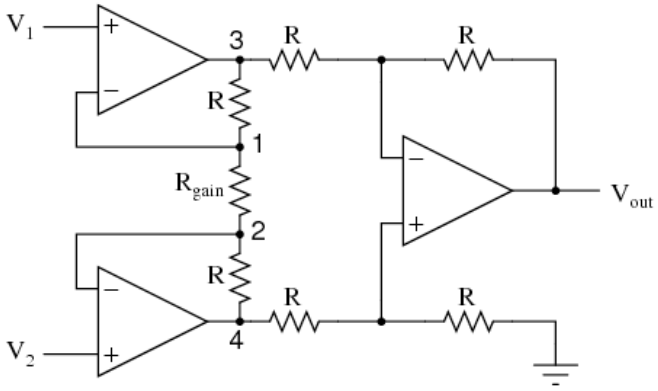


Performing a frequency analysis shows the loss relative to the source. A 6dB loss of signal voltage comes from the 50 ohm resistor which has been included for simulation integrity.



The frequency response and overall loss looks realistic of a real world situation.

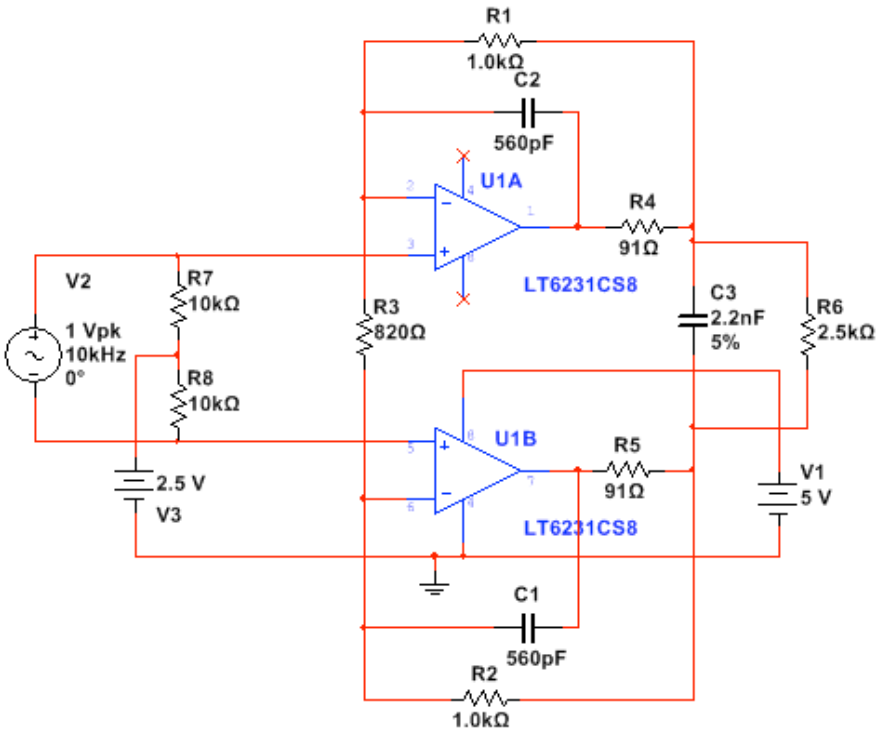
Moving on, the QSD in the planned configuration requires a differential amplifier. It is easy to get an unbalanced signal from balanced, but not so easy to to back the other way. The classic design is shown next:



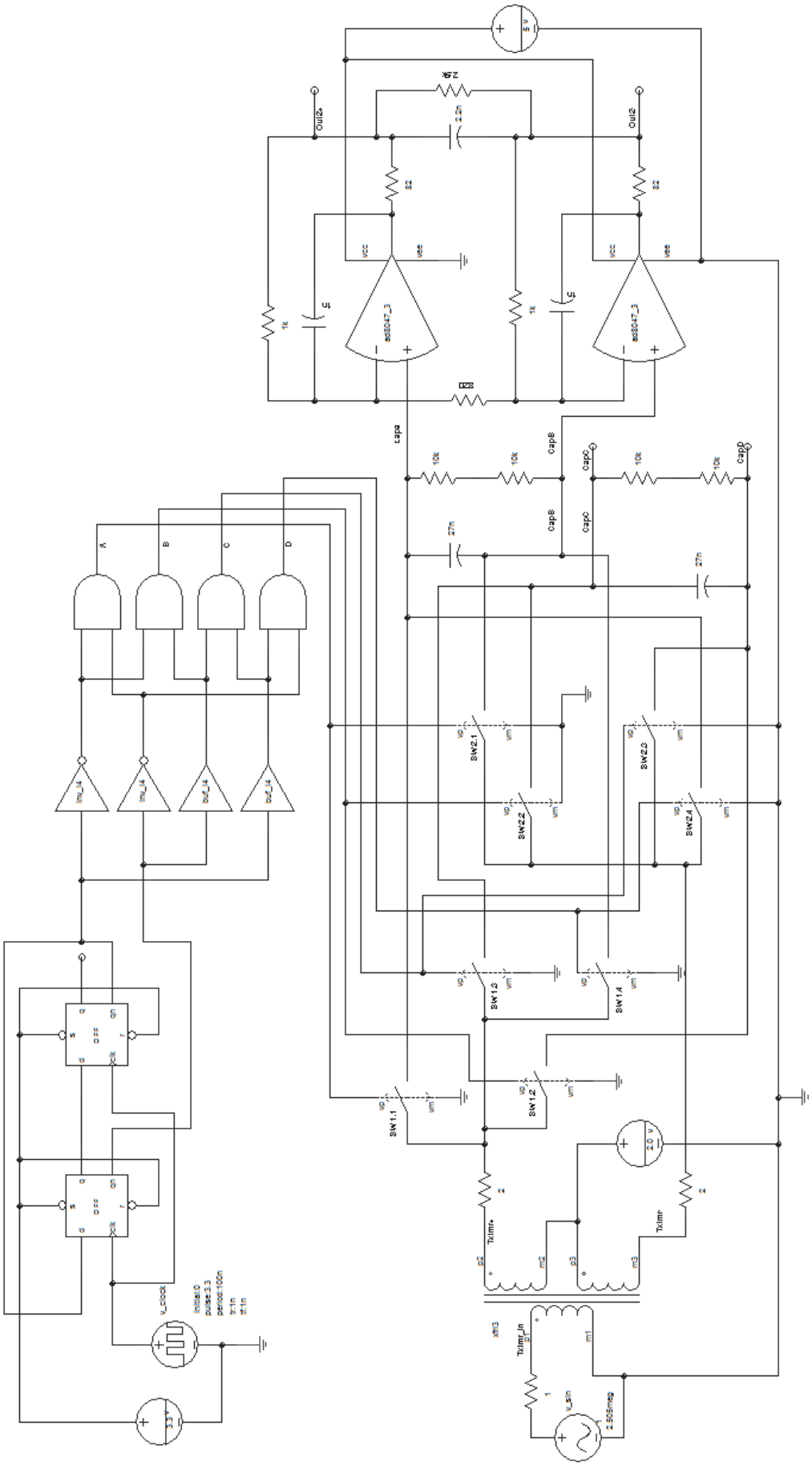
Saber does not contain the LT6237 model, which is too new. Attempts to convert the Linear Tech SPICE model into a Saber MAST model failed. As a rough check I used an OP297 model. Initially I was interested in a quick confirmation of the gain. The circuit above does indeed have a differential voltage gain of 3x. Another useful result is looking at the input voltage to the op-amps. With 0.5v p-p input signals, the actual amplifier inputs only register 30mV differentially. Just as well because these devices have back to back protection diodes only allowing 0.7V swing.

Further attempts to get a MAST model of the LT6231/LT6237 failed. The SPICE model convert tool in Saber is poor in my opinion. So I started to model the differential amplifier in another simulator. The circuit recommended by 24-bit ADC manufacturers is a variation of the classic differential amp, with first order-lowpass and another pole thrown in the differential path.

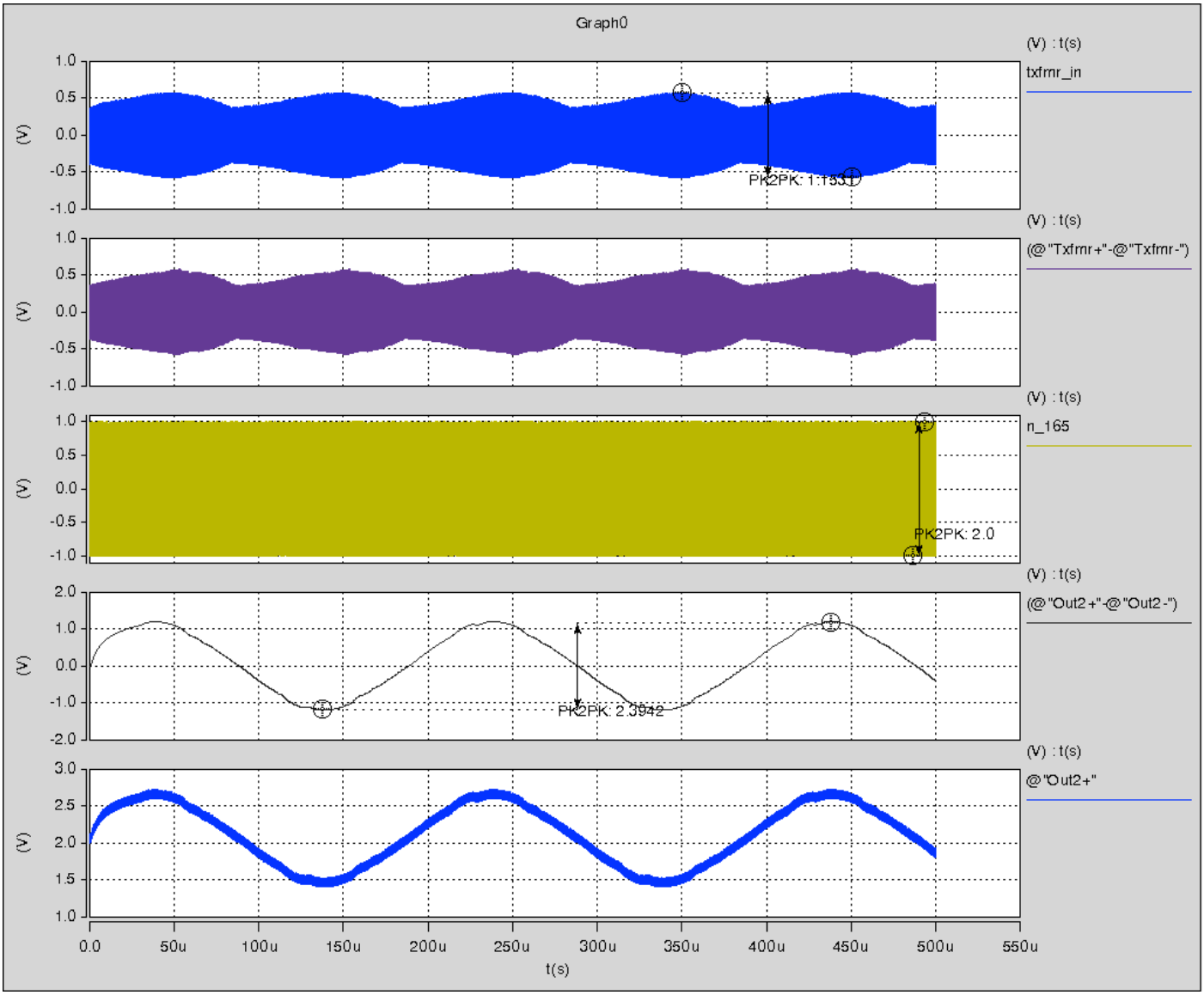
The amplifier has to start rolling off (~0.5dB) at 192kHz. I found the circuit given by Asahi Kasei AK5394A and Cirrus Logic CS5381 data-sheets works, but the roll-off is not at 192kHz. I cannot find the input impedance of the AK5394, but the CS5381 data gives 2.5k, so used that.



The whole simulation circuit then becomes:



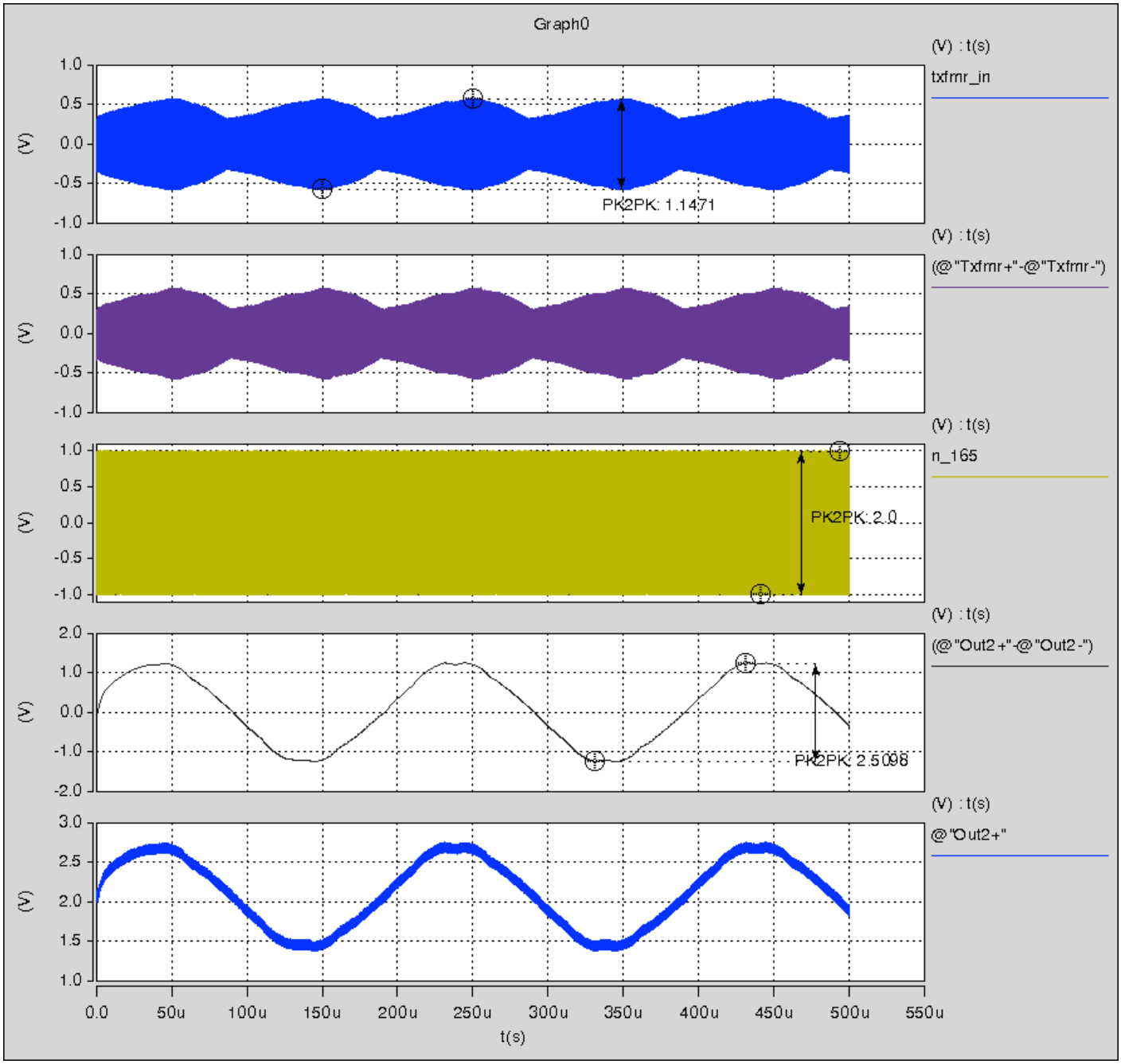
Next to examine the effect of linearity swamping resistors, and switch resistance on amplitude. Putting in 10 ohms and 5.6 for the resistors shows there is a difference, but not huge.



Regarding the differential output signal, it is 2.39V p-p on this graph. The input signal is +/- 1.0V (2.0V p-p). Signal frequencies simulated are 2.505MHz input signal and 10.0MHz local oscillator. To produce the 5.0kHz output signal on the second trace from bottom.

The bottom trace indicates the actual (non-differential) output of the op-amp is a decent way from hitting the supply rails. Simulation helps a lot with predicting how much headroom there will be on the amplifiers.

The top 2 traces indicate there is some modulation of the input signal by the output signal. This must be present on all QSD implementations, so it can't be a big problem. Looking at why this occurs, it is from AM modulation of the low frequency output going back through the switches. Nothing to do with having the circuit unbalanced. After several experiments failed, I am now at a loss to see how to remove this effect. It can be reduced by increasing the linearity swamping resistors, but of course that increases the conversion loss too. We see that

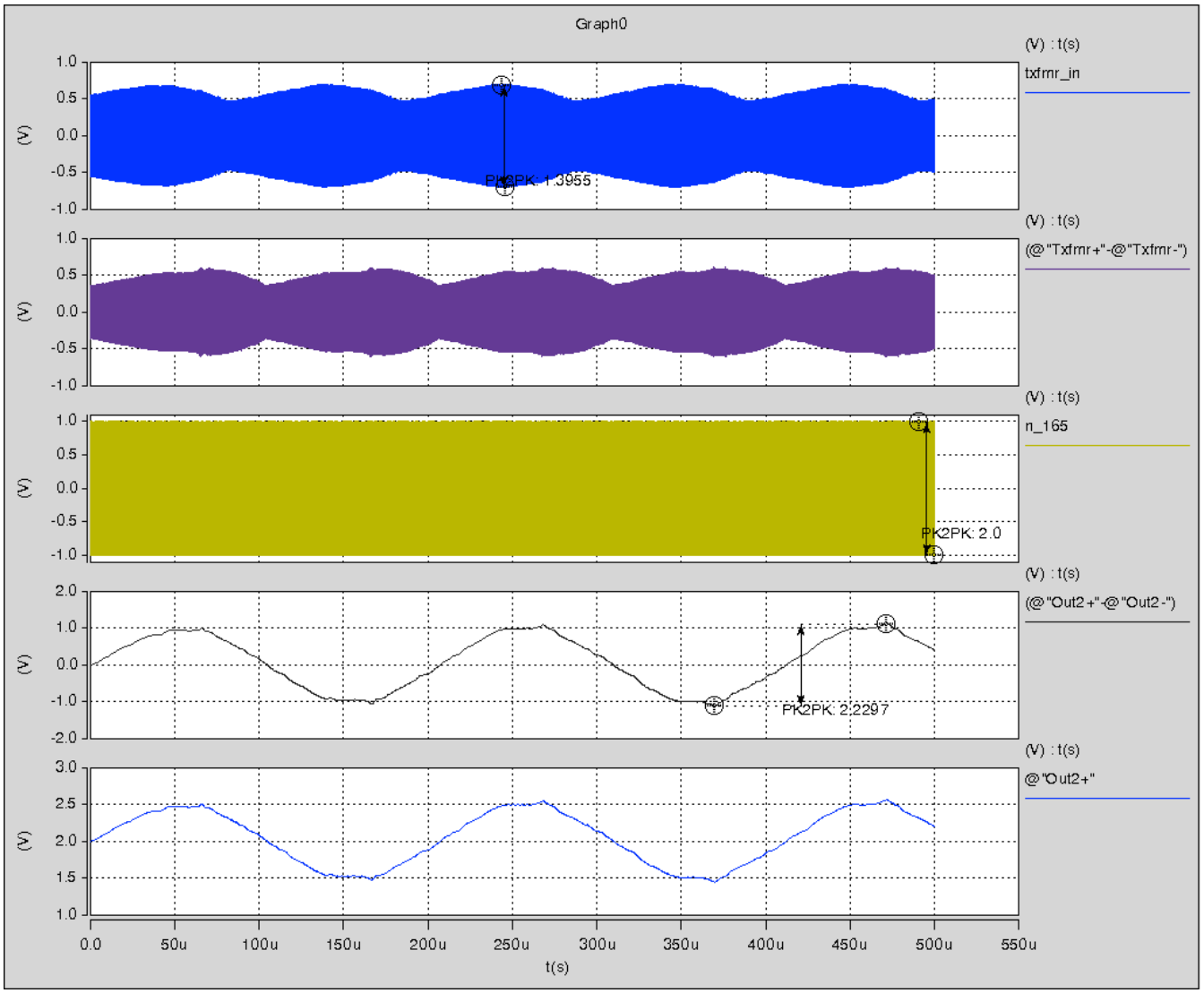


changing swamping resistors from 10 to 5.6 ohms increases output signal by 2.39 to 2.51V. I would rather leave them at 10 ohms because output distortion is worse with lower values.

Another question is how the output signal level varies with frequency. I ran the simulation with 30.005MHz and 120MHz signals. Using 10 ohm resistors. The signal has dropped to 2.2V p-p of which some is due to the transformer and some the characteristics of the analog switches and digital circuit. Note the slight distortion of the output signal has increased at the higher frequency simulation.

I did not go far down the road of experimenting with different switching times. Saber allows switching thresholds of the analog switches to be set, simulating the break-before-make effect of CMOS switches. As I intend to use CMOS type switches in the final circuit, it seemed unnecessary to try and simulate NMOS. Which is harder to do anyway.

The next graph is the effect of increasing the swamping resistors back to 10 ohms.

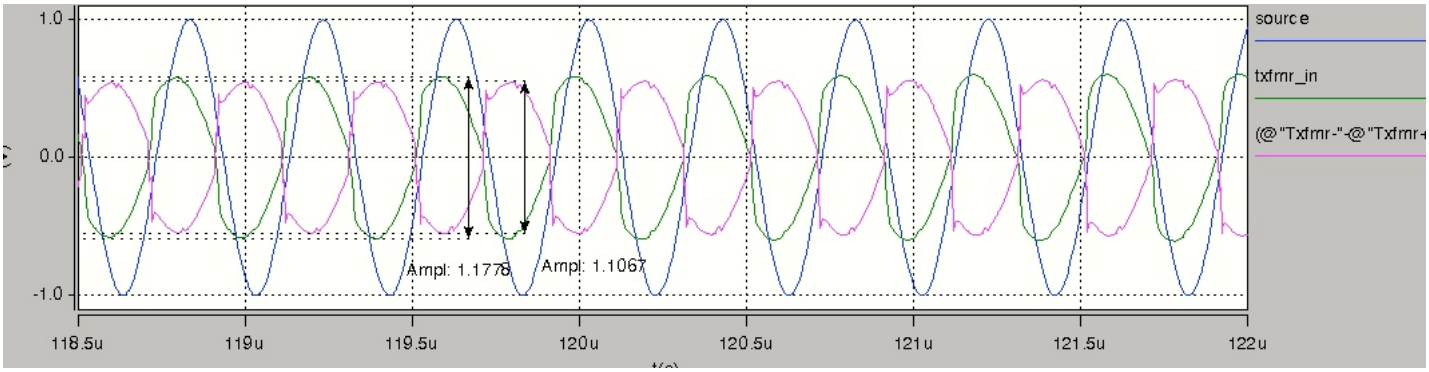


The output signal has dropped a bit as expected.

5. Looking into the input.

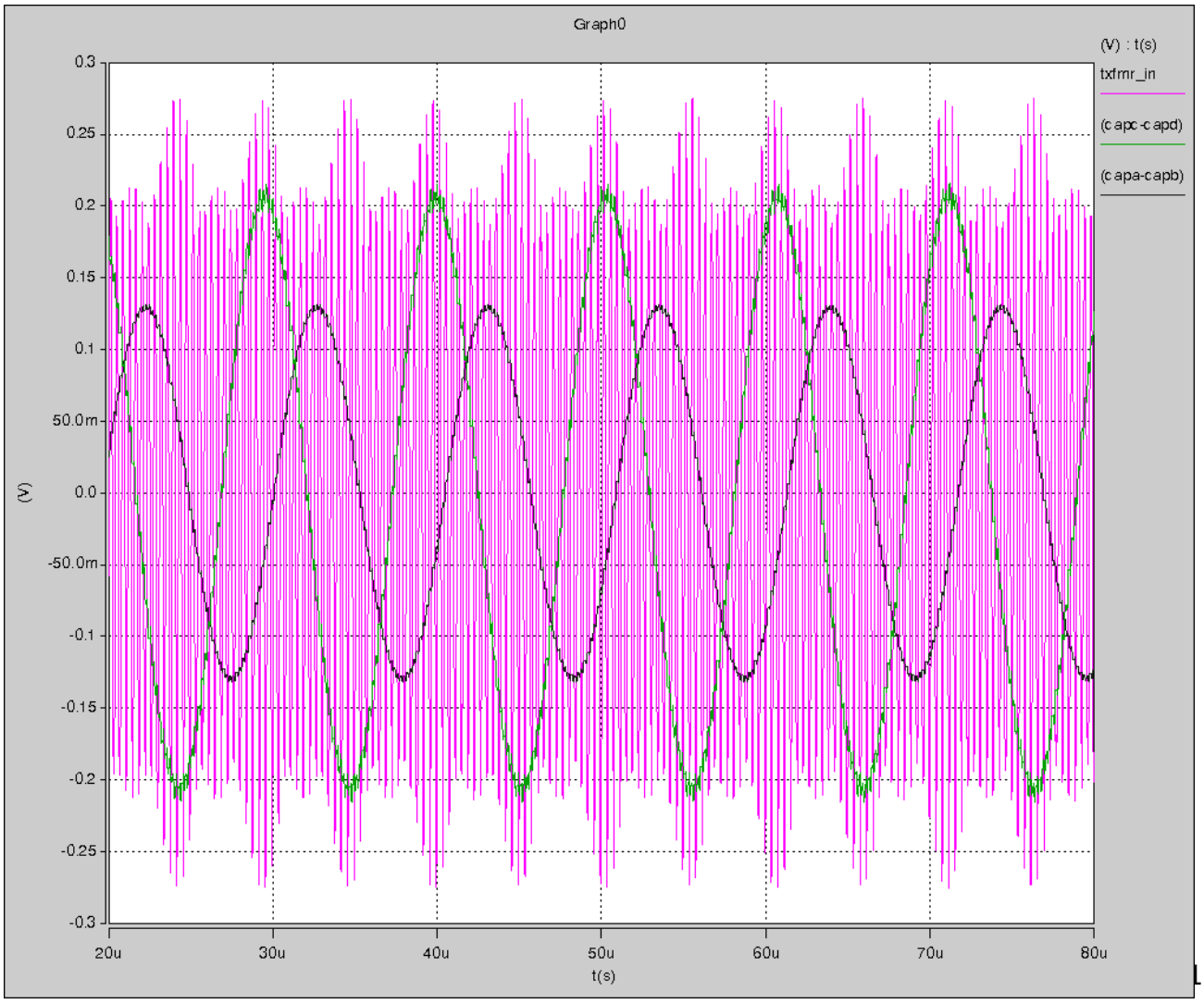
The final job is to get a measurement of the input impedance. There are tools in Saber for RF type measurements (S parameter, etc.) but at the moment I do not know how to access them. It is possible to estimate the input impedance by using a simple voltage divider law. Unfortunately the input signal gets modulated by the output, so I guess that 50% level of the signals will give the best estimate.

Input voltage of 2.0V p-p and voltage at the transformer input of 1.18V gives impedance of 72 ohms. changing the transformer ratio is the obvious way to get the input impedance down. With 12 turn primary and 7+7 secondary, the match looks better. The simulation shows the output voltage barely changes, probably the switch losses coming into play. The transformer input voltage dropped to 1.03V, indicating a good 50 ohm match.



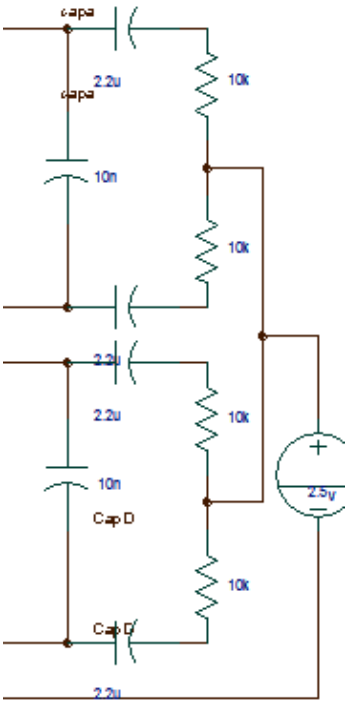
6. Sampling capacitor value

I think the receiver needs at least 96kHz bandwidth, some people use 192kHz. The values of the sampling caps will attenuate the higher frequencies if they are too big. The optimum value is around 10nF. The next plot shows a 96kHz IF signal with 27nF(black trace) and 10nF(green).



7. Post Switch Amplifier

The most economical implementation is with dual op-amps. They are cheaper than instrumentation amplifiers of the same performance. The post switch amplifier has to be as low-noise as possible, low current, be a low-pass filter, and provide enough gain to overcome any possible front end losses.

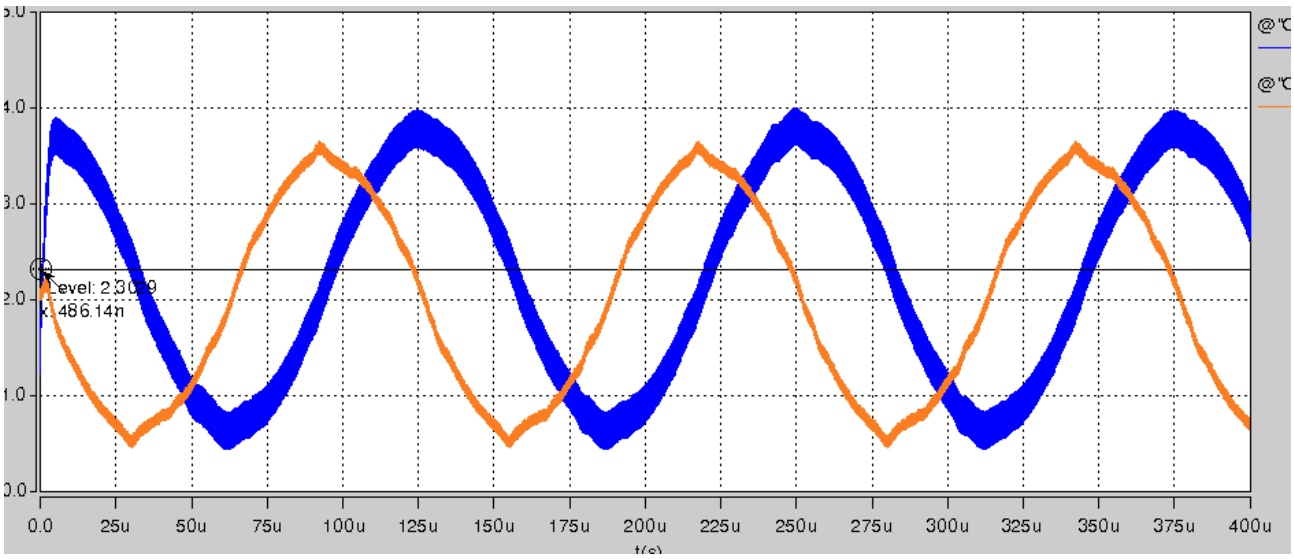


Most QSD SDR designs have a large gain at the post switch amplifier. Having large gain improves sensitivity with 16-bit ADCs. But if the following ADC is very low noise, a high gain is not required. With a 24-bit ADC, the low noise floor can be utilised to help improve dynamic range. Having low gain at the post switch amplifier improves dynamic range as the stage will not clip. The limitation on performance then falls on the ADC, which with 24-bit is excellent.

A starting value for gain of the amplifier is x3. Experimentation will be required on the physical circuit to determine the optimum gain, which will probably be greater than x3.

The bias point for the switches will be below half supply. In the simulations it is 2.0V. Therefore there is an offset in the output signals, causing them to clip on the lower edge. Previous QSD designs used capacitors ahead of the amplifier, and voltage dividers to set mid-rail output levels. As in the circuit shown left.

Its possible to remove the capacitors and use resistors to move the amplifier outputs closer to mid-rail. This saves at least 4 capacitors and probably 2 resistors. The last plot of this report shows how the offsetting resistors move the blue trace closer to mid-rail, further optimising dynamic range. The gain is also slightly increased as an innocuous side effect.



8. Implementation and Conclusions

After a lengthy survey of 4:1 multiplexers and op-amps, I settled on TS3A5017 (TI) and LT6237 (Linear). The TS3A5017 is a CMOS switch, with better specs than the FST bus switches, except slightly slower switching speed. The higher supply voltage reduces the on-resistance. The chip is footprint compatible with others, including NMOS bus switches.
To get a differential output the LT6237 with classic instrumentation amp circuit is ideal for 1-4V input ADC devices such as AK5394 and is cheap.
As said in the intro, I am doing this project for myself, and it will be orientated towards SDR specific "soundcards" that have 1-4V ADC chips. So the implementation will be with the LT6237, which is a familiar part for Softrock people, as the older LT6231 was used in that.
The proof of all this is in hardware, but I'm sure this design is better than the Softrock mixer. Simulation shows voltage on switches is about ½ of input amplitude. So 3V3 switches will not clip, even with 5V powered switches in preceding stages. CMOS multiplexers on the market have max supply of 4V.

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